

**REMARKS**

In this Amendment, claims 1 and 9 are amended, claims 2-3, 7-8, 10-11 and 15-16 are cancelled. Claims 1 and 9 are the independent claims, and claims 1, 4-6, 9 and 12-14 remain pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

The object of the present invention is to control the OFF-state leakage current and the ON-state current by setting a gate threshold voltage to an appropriate value (that is, approximately 0.36 V in the embodiment). This is described at page 12, lines 26-32 in the specification, for example. The appropriate value of the gate threshold voltage is determined on the basis of both the OFF-state leakage current and the ON-state current. When the gate threshold voltage is high, the OFF-state leakage current becomes low, but the ON-state current also becomes low. This leads to a problem that an operational speed of the semiconductor device decreases. This is described in the specification at page 9, lines 16-21. The appropriate value of the gate threshold voltage is determined as described above, and it is desirable that the appropriate value of the gate threshold voltage be approximately 0.36 V.

To realize such appropriate value of the gate threshold voltage, it is necessary that the semiconductor device of the present invention satisfies the following conditions (1) to (3):

- (1) the conductivity type of the gate electrode is P-type, and the conductivity type of the channel is N-type;
- (2) the impurity concentration in the channel is approximately from  $3 \times 10^{17}$   $\text{cm}^{-3}$ ; and

(3) a channel length of the channel is approximately  $0.15\ \mu\text{m}$ .

In other words, the gate threshold voltage is decreased by satisfying the condition (1) "the conductivity type of the gate electrode is P-type and the conductivity type of the channel is N-type" and the condition (2) "the impurity concentration in the channel is approximately from  $3 \times 10^{17}\ \text{cm}^{-3}$ ." This is described in page 7, line 29 - page 8, line 6 in the specification and in FIG. 3 as the gate threshold voltages T0 (example for comparison) and T1 (embodiment). See also the paragraph bridging pages 5 and 6. The gate threshold voltage is further decreased to be an appropriate value, approximately 0.36 V, by also satisfying the condition (3) "a channel length of the channel is approximately  $0.15\ \mu\text{m}$ ." This is described in page 8, lines 7-25 in the specification.

As described above, the effects of the present invention can be obtained only when all of the conditions (1), (2), (3) (that is, a combination of all of the conditions (1), (2), (3)) are satisfied.

In contrast to this, the Examiner states that Nathanson discloses the condition (1) and the condition (3), Yamazaki discloses MOSFET wherein the first and second n-channel transistors wherein the area under the source and drain have an impurity concentration of  $1 \times 10^{20}$  to  $1 \times 10^{21}\ \text{cm}^{-3}$ , Kao discloses a n-channel/n-source/n-drain MOSFET wherein the channel impurity concentration is approximately  $3 \times 10^{17}\ \text{cm}^{-3}$ , and it is obvious to have used Yamazaki's/Kao's higher impurity concentration in Nathanson's device.

However, Kao does not disclose a channel impurity concentration of approximately  $3 \times 10^{17}\ \text{cm}^{-3}$ , but disclose an impurity concentration of  $5 \times 10^{17}$  to  $1 \times 10^{18}\ \text{cm}^{-3}$ , as shown in Col. 4, line 32.

Furthermore, none of the cited references discloses or even suggests that the technology disclosed in Yamazaki's or Kao's impurity concentrations can be used in the technology disclosed in the Nathanson (i.e., the Nathanson's device). Thus, the applicant believes that it is not obvious to combine the cited references.

In addition, even supposing that the combination of the cited references was possible, the condition (2) "the impurity concentration in the channel is approximately from  $3 \times 10^{17} \text{ cm}^{-3}$ " is not disclosed or suggested in any of the cited references.

Based on the above, it is submitted that this application is in condition for allowance and such a Notice, with allowed claims 1, 4-6, 9 and 12-14, earnestly is solicited.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

No fee is believed due. Should any fee be required, however, the Commissioner is hereby authorized to charge the fee to our Deposit Account No. 18-0002, and advise us accordingly.

Respectfully submitted,



Steven M. Rabin – Reg. No. 29,102  
RABIN & BERDO, PC  
Cust. No. 23995  
Facsimile: 202-408-0924  
Telephone: 202-371-8976

June 30, 2008  
Date

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AMENDMENT

10/690,579